

WHAT IS CLAIMED IS:

- 1 1. A method of designing a phase shifting mask, the method
2 comprising:
 - 3 identifying edges of a first phase region of a phase shifting
 - 4 mask, the first phase region being located proximate a critical region and
 - 5 the identified edges not being edges of the first phase region adjacent to
 - 6 the critical region;
 - 7 expanding the identified edges to define a narrow line along
 - 8 the edges of the first phase region; and
 - 9 forming chrome in the narrow line to form a chrome
 - 10 boundary along the edges of the first phase region.
- 1 2. The method of claim 1, wherein forming chrome in the
2 narrow line to form a chrome boundary includes merging the narrow line
3 with a chrome database.
- 1 3. The method of claim 1, further comprising:
 - 2 assigning phase polarities to the first phase region;
 - 3 defining edges of the first phase region;
 - 4 establishing a boundary around the defined edges; and
 - 5 assigning area outside of the established boundary to have
 - 6 phase zero.
- 1 4. The method of claim 3, wherein the first phase region and a
2 second phase region are assigned phase angles 180 degrees from each
3 other.
- 1 5. The method of claim 4, further comprising generating a trim
2 mask to remove undesired patterns between the first phase region and
3 the second phase region.

1 6. The method of claim 1, wherein the narrow line has a width
2 of a minimum gate width dimension.

1 7. The method of claim 1, further comprising defining a
2 boundary around the critical region.

1 8. The method of claim 7, wherein defining the boundary
2 includes defining a boundary around edges having phase 180.

1 9. The method of claim 1, further comprising defining break
2 locations to have minimal impact on circuit performance and yield.

1 10. The method of claim 9, wherein the break locations have a
2 width that permits patterning and inspection.

1 11. The method of claim 1, further comprising generating a trim
2 mask to remove undesired patterns between regions of first and second
3 phases.

1 12. A method of generating phase shifting patterns to improve
2 the patterning of gates and other layers needing sub-nominal dimensions,
3 the method comprising:

4 defining critical gate areas;
5 creating phase areas on either side of the critical gate areas;
6 assigning opposite phase polarities to the phase areas on
7 either side of the critical gate areas;
8 enhancing phase areas with assigned phase polarities;
9 defining break regions where phase transitions are likely to
10 occur;
11 generating polygons to define other edges and excluding the
12 defined break regions; and

13 constructing a boundary region outside of first phase regions
14 to form a chrome border.

1 13. The method of claim 12, further comprising:
2 correcting design rule violations; and
3 applying optical proximity and process corrections to phase
4 regions to allow proper pattern generation.

1 14. The method of claim 12, further comprising generating a trim
2 mask to remove undesired patterns between first phase regions and
3 second phase regions outside of a desired pattern.

1 15. The method of claim 14, wherein the generating is done by
2 oversizing boundary and break regions.

1 16. The method of claim 14, wherein the chrome border has a
2 width of a distance between phase 0 and phase 180 regions.

1 17. A method of enhancing clear field phase shift masks with a
2 chrome border around outside edges of a first phase area, the method
3 comprising:

4 assigning phase polarities to phase areas, the phase areas
5 including first phase areas and second phase areas;
6 defining edges of the assigned phase areas;
7 establishing a boundary around the defined edges of the first
8 phase areas; and
9 forming a chrome border in the boundary around the first
10 phase area.

1 18. The method of claim 17, wherein defining edges of the
2 assigned phase areas includes defining break regions where phase
3 transitions occur and generating polygons including edges but excluding

4 break regions, wherein the polygons are merged with the assigned phase
5 areas.

1 19.1 The method of claim 17, further comprising generating a trim
2 mask to remove undesired patterns between the first phase area and the
3 second phase area.

1 20. The method of claim 19, wherein the generating is done by
2 oversizing the boundary and break regions.

1 21. A mask configured for use in an integrated circuit
2 manufacturing process, the mask comprising:
3 a critical pattern section defined by first edges of a phase
4 zero region and first edges of a phase 180 region; and
5 a chrome boundary region located outside second edges of
6 the phase 180 region, the second edges of the phase 180 region being
7 different than the first edges of the phase 180 region, wherein the
8 chrome boundary region includes an opaque material.

1 22. The mask of claim 21, further comprising a region outside of
2 defined areas having a phase of zero.

1 23. The mask of claim 21, wherein the opaque material includes
2 chrome.

1 24. The mask of claim 21, wherein the phase zero region and the
2 phase 180 region are assigned phase angles 180 degrees from each
3 other.